# Enhanced Charge Injection Through Nanostructured Electrodes for Organic Field Effect Transistors

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**Nanosphere lithography is used to process nanopore-structured electrodes, which are applied into the fabrication of bottom-gate, bottom-contact configuration organic field effect transistors (OFETs) to serve as source/drain elecrodes. The introduction of this nanopore-structure electrode facilitates the forming of nanopore-structure pentacene layers with small grain boundaries at the electrode interface, and then reduces the contact resistance, contact-induces the growth of pentacene and accordingly improves the mobility of charge carriers in the OFETs about 20 times as compared with results in literature through enhancing the charge carrier injection. It is believed that this structure of electrode is a valuable approach for improving organic filed effect transistors.**

fabricating the OFETs. The introduction of these nanopore-structure electrodes tremendously improves the grain structure of the semiconductor to form nanopore structure at the electrode interface. The existing of nanopore-structure semiconductor reduces the contact resistance, contact-induces the growth of pentacene in the region of the channel close to the electrode and accordingly enhances charge carrier injection, resulting in improving the mobility of charge carriers in the OFETs about 20 times as compared with results in literature.

## 1. Introduction

Organic field effect transistors (OFETs) are considered as a promising cost-effective alternative to silicon-based transistors in a variety of applications.[1] Significant progress has been achieved in the development of novel semiconductor materials and device structures for high performance devices in the last decade.[2] It is noted that processing organic circuits is an inevitable trend in the development of organic field effect transistors.[3] Here, bottom-gate, bottom-contact (BGBC) configuration OFETs is considered due to its simple processing to manufacture organic circuits. It has been discussed that BGBC devices intrinsically possess a smaller injection area and disadvantageous injection path compared with top-contact devices.[4] Therefore, it is a key point to effectively enhance charge injection in the BGBC configuration. The enhancements of charge injection in the BGBC configuration are available by several methods such as electrode modification,[5] short channel electrodes[6] and interface engineering.[7] The former is to tune the work function of the metal for favorable charge injection. The latter two approaches are reducing the grain boundaries between the channels for less charge trapped in these defects. In our work, nanosphere lithography was used to produce nanopore-structured source/drain electrodes in the process of

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## 2. Results and Discussion

### 2.1. Nanopore-Structured Source/Drain Electrodes Via Nanosphere Lithography

The use of nanosphere lithography is an attractive approach to manufacture nanopore structures,[8] which recently have gained increasing attention in organic electronics [9] because of its controllable size, simplicity of operation and effortless remove. **Figure 1** schematically illustrates our experimental design for the process of nanopore-structured source/drain electrodes via nanosphere lithography. First, a large-area and close-packed monolayer of polystyrene nanospheres (diameter, 600 nm) was formed on the surface of deionized water with the help of sodium dodecyl sulfate (SDS) (Figure 1a). Second, a cleaned Si wafer coated with 300 nm thermal oxide layer was immersed into the deionized water (Figure 1b) and transferred the monolayer onto its surface (Figure 1c). An $O_2$ plasma treatment was then utilized to etch the polystyrene nanospheres (Figure 1d). It should be noted that the size of polystyrene nanospheres can easily be controlled by different etching time or power. Next, metal layers including a 3 nm chrome (adhesion layer) and a 15 nm gold layer were deposited through metal mask (Figure 1e). Subsequently, the nanopore-structured electrodes (Figure 1f) were finished after dissolving away the polystyrene nanospheres wiht acetone. Figure S1a, Supporting Information, shows a scanning electron microscopy (SEM) image of a close-packed monolayer of PS nanospheres with a diameter of 600 nm. The size of PS nanospheres can be well controlled by tuning the treatment time (inset of Figure S1a, Supporting Information). 500 nm (Figure S1b, Supporting Information), 400 nm (Figure S1c, Supporting Information), and 300 nm (Figure S1d, Supporting Information), diameter PS nanospheres were produced using

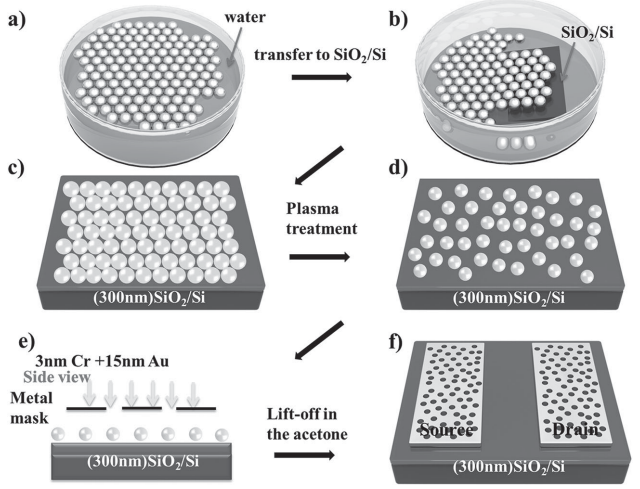


**Figure 1.** a) Large area monolayer of polystyrene nanospheres on the deionized water. b) Transfer the polystyrene nanospheres onto $SiO_2$/Si. c) Monolayer of polystyrene nanospheres on $SiO_2$/Si. d) Separated polystyrene nanospheres on $SiO_2$/Si. e) Deposit the metal through mask. f) Lift off the polystyrene nanospheres in the acetone.

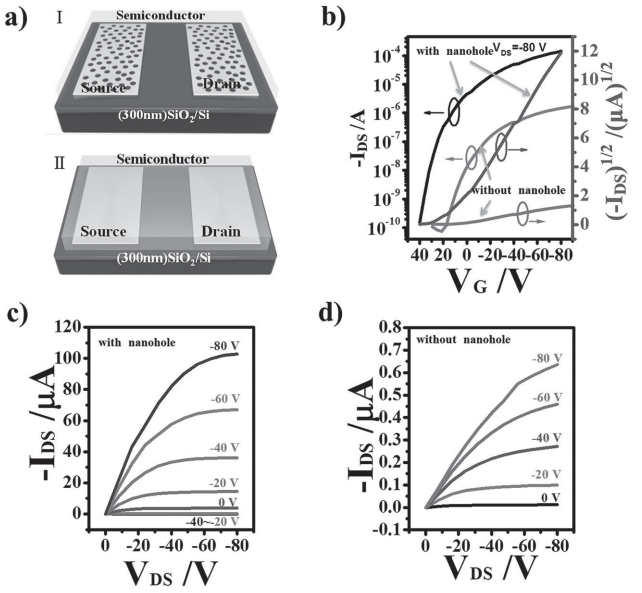


**Figure 2.** a) The structure of OFET with (I) and without (II) nanopore-structured electrodes. b) Typical transfer characteristics of the transistor based on source/drain electrodes with and without nanopore structure. c) Typical output characteristics of the transistor based on source/drain electrodes with nanopore structure. d) Typical output characteristics of the transistor based on source/drain electrodes without nanopore structure.

this method. Large area (20 × 20 μm) atomic force microscope (AFM) images of nanopore-structured electrodes are shown in Figure S2, Supporting Information. They display that the lift-off place was clean. The diameter of the nanopore structures in the source/drain electrodes was 500 nm (Figure S2b, Supporting Information), 400 nm (Figure S2c, Supporting Information), and 300 nm (Figure S2d, Supporting Information), respectively.

### 2.2. OFETs Fabrication and Measurements

Here we discuss experiments done on 400 nm nanopore-structured source/drain electrodes (**Figure 2**a,I) as an example and a system without nanopore-structured electrodes (Figure 2a,II) for comparison. A scheme of an OFET with 30 nm pentacene as an active layer is shown in Figure 2a. Figure 2b showed the transfer electrical characteristics of the device with and without nanopore structure under the same conditions. The device without nanopore structure shows a mobility calculated from saturation region of the transfer curve of about 0.01 $cm^2\ V^{-1}\ s^{-1}$, which was comparable with results of the previous reports [10] of our lab. Indeed, higher performance was observed from the device with nanopore structures with a mobility of 0.22 $cm^2\ V^{-1}\ s^{-1}$. Both of these two kinds of devices showed the expected gate modulation of the drain current ($I_D$) in both the linear and saturation regimes (Figure 2c,d). A multitude of devices with the same channel width (1000 μm) and different channel length (40, 55, 70, 90, and 125 μm) were investigated and the statistical data is shown in Figure S3, Supporting Information. The maximal current of the devices without nanopore structure maintained at a low level (2.6–4.6 μA) (Figure S3a, Supporting Information). From Figure S3b, Supporting Information, it could be seen that the nanopore structure allowed increasing the maximal current up to 160 μA (Figure S3b, Supporting Information), which is an improvement by a factor of 38 (Figure S3c, Supporting Information). Obviously, the nanopore structure enhanced the charge injection significantly and thus increased the maximum current. Other nanopore structures, such as 300 and 500 nm, likewise improved the corresponding performance of these devices with different channel length, and were summarized in Figure S4a, Supporting Information.

Furthermore, with increasing nanohole area percentage covering the electrode (Figure S4b, Supporting Information), the average mobility distinctly increased. The highest mobility of the device calculated from the saturation region of the transfer curve was 0.46 $cm^2\ V^{-1}\ s^{-1}$ based on 500 nm nanopore structures (Figure S4a, Supporting Information).

### 2.3. Characterization of Morphology and Contact Resistance

The morphological characteristics of pentacene thin films on the interface were examined next. As shown in the AFM images of the morphology of pentacene on the surface of gold with nanopore structure, large-area (20 μm × 20 μm) nanopore-structured pentacene (**Figure 3**a–c) was observed covering on the whole gold surface. In addition, the size of nanopore-structured pentacene could also be controlled (such as 500, 400, and 300 nm) based on the nanopore-structured gold electrode. As seen at the higher magnification AFM image (5 μm × 5 μm) (Figure 3d–f), the nanopore-structured pentacene displays fewer grain boundaries compared with pentacene on the gold without the nanopore structure, which

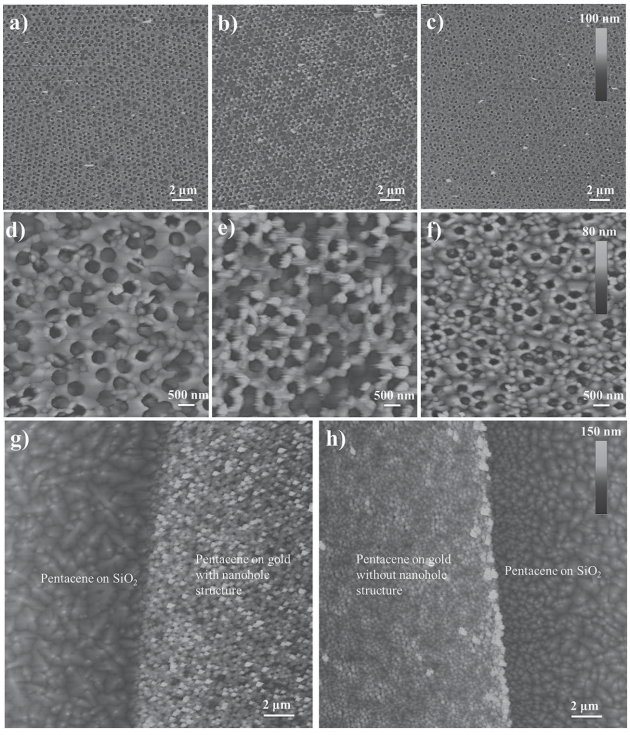


**Figure 3.** Large-area (20 μm × 20 μm) AFM images of the morphology of pentacene on the gold surface with a) 500 nm nanopore structure, b) 400 nm nanopore structure, c) and 300 nm nanopore structure. Amplification (5 μm × 5 μm) AFM images of the morphology of pentacene on the gold surface with d) 500 nm nanopore structure, e) 400 nm nanopore structure, and f) 300 nm nanopore structure. g) The morphology of pentacene on the electrode with nanopore structured, $SiO_2$ surface and the contact interface. h) The morphology of pentacene on the electrode without nanopore structured, $SiO_2$ surface and the contact interface.

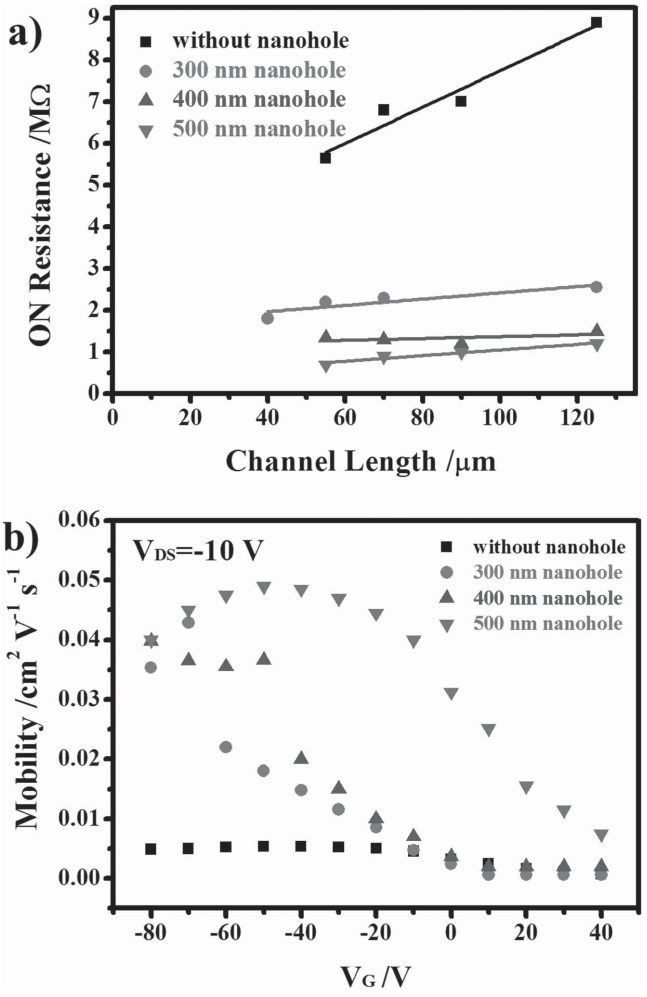


**Figure 4.** a) Plots of channel length versus resistance of devices with different nanopore structure. b) Gate–voltage dependent mobility of different nanopore structure.

was consistent with previous reports.[11] Besides, it was found that this nanopore-structured pentacene layers still affected the growth of pentacene on the insulator ($SiO_2$) contacting with the gold. As shown in Figure 3g,h, the grain size of pentacene molecule contact-induced[12] of the interface area by nanopore structure (Figure 3g) was clearly larger than that without the nanopore structure (Figure 3h), which facilitated the charge injection from the electrode into the semiconductor. We further estimated the contact resistance between the electrodes and semiconductor and the channel mobility on the basis of previous literature reports.[13,14] There a low source–drain voltage ($V_{DS}$ = –10 V) from the linear region of the OFET was selected in this measurement. **Figure 4**a shows a plot of $R_{ON}$ as a function of $L$ at the gate voltage of –80 V. The contact resistances of our nanopore structures (including 500 nm: 0.5 MΩ, 400 nm: 1.2 MΩ, 300 nm: 1.6 MΩ) were lower than that without nanopore structures (3.4 MΩ). Figure 4b shows the gate–voltage dependent mobility, which demonstrates the nanopore structure indeed enhance channel mobility. Both of these above-mentioned tests confirmed that the introduction of nanopore structures decreased the contact resistance to improve the carrier injection effectively, and this was helpful in the enhancement of field-effect mobility.

### 2.4. Growth Mode of Pentacene Molecule

Plasma treatment was also a crucial factor for the growth of nanopore structure of pentacene prior to sequential evaporation of pentacene on the surface of gold. **Figure 5**a,b shows the growth model of the pentacene molecule on the gold surface without and with plasma treatment, respectively. It was found that pentacene molecules only grew on the surface of gold without plasma treatment at the beginning of a few (5 nm) layers (Figure 5c) and the morphology of pentacene appeared as a long striped structure, which arranged randomly. However, pentacene molecules existed on both surfaces of gold and insulator (Figure 5e) with plasma treatment and the distribution of the molecules was very homogeneous. With increasing thickness of pentacene molecular layers up to 10 nm, the growth became obviously different. For the growth of pentacene molecules on the surface without plasma treatment, the trend of molecular aggregation was obvious and the long striped structures gradually covered all the nanopore of gold (Figure 5d), resulting in no effect on the charge injection. Therefore, the performance of this device was the same with that without nanopore-structured

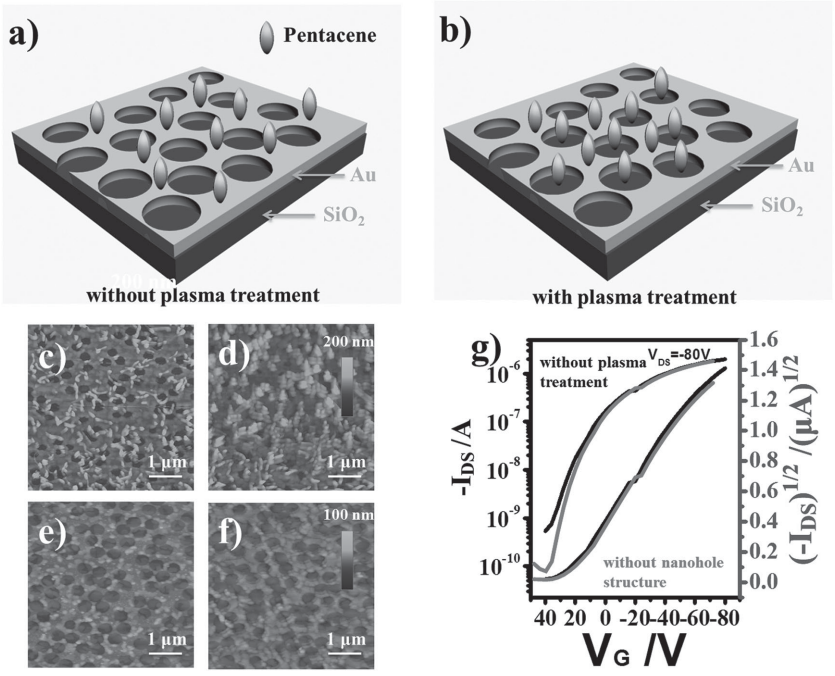


**Figure 5.** a) Growth model of pentacene molecule on the surface without plasma treatment. b) Growth model of pentacene molecule on the surface with plasma treatment. c) 5 nm pentacene on the surface without plasma treatment. d) 10 nm pentacene on the surface without plasma treatment. e) 5 nm pentacene on the surface with plasma treatment. f) 10 nm pentacene on the surface with plasma treatment. g) Typical transfer characteristics of the transistor based on nanopore-structure electrode without plasma treatment and without nanopore-structured electrode.

source/drain electrodes (Figure 5g). This demonstrated that nanopore-structured pentacene was only formed (Figure 5f) on the nanohole-structure surface with plasma treatment and the nanopore structure was of great importance for the enhancement of charge injection. The possible charge transportation mechanism with this nanopore structure was deduced as follows: It is known that charge is injected from the source electrode and charge transfer occurs through the interface between the insulator and semiconductor.[15] When nanopore structures existed in the electrode, they facilitate the forming of nanopore-structure pentacene layers with small grain boundaries at the electrode interface. Subsequently, the existing of nanopore-structure pentacene not only reduced the contact resistance, but also affected the growth of semiconductor along the contact between the electrode and the insulator. This effectiveness tremendously enhanced charge carrier injection and then further improved the performance of the device.

## 3. Conclusion

In conclusion, BGBC configuration OFETs are primarily considered in the process of manufacturing the organic circuits due to its simple processing to manufacture organic circuits. Here, nanopore-structured source/drain electrodes applied into the BGBC configuration OFETs are fabricated by nanosphere lithography. The introduction of this nanopore-structure electrode facilitates the forming of nanopore-structure pentacene layers with small grain boundaries at the electrode interface, and then reduces the contact resistance, contact-induces the growth of pentacene and further enhances the charge injection from the source electrode into the interface for higher performance. It is believed that this structure of electrode is a valuable approach for improving organic filed effect transistors.

## 4. Experimental Section

*Materials and Instruments*: Pentacene, polystyrene monodisperse nanospheres and sodium dodecyl sulfate were purchased from Sigma-Aldrich. Pentacene was used as received without further purification. Silicon wafers with 300 nm thermally oxidized $SiO_2$ layer were purchased from Si-mat Company. Silicon wafers with 300 nm thermally oxidized $SiO_2$ layer used in the present study were successively cleaned with deionized water, acetone, pure ethanol, piranha solution ($H_2SO_4$:$H_2O_2$ = 7:3), deionized water, and isopropanol. Atomic force microscopy measurements were carried out on a Multimode Nanoscope IIIa instrument (Digital Instrument) in tapping mode with silicon cantilevers. Scanning electron microscopy was performed on a LEO VP 1530 field emission system. Metal deposition was carried out in a vacuum chamber using W wire as heating source under a vacuum of $10^{-4}$ Pa. Semiconductor deposition was performed in a home-designed vacuum system under $10^{-6}$ Pa. The electrical characteristics of the OFET devices were recorded at room temperature in air by using a Keithley 4200 SCS semiconductor parameter analyzer and a Micromanipulator 6150 probe station.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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